

A SYMMETRICAL STACKED INDUCTOR

Background of the Invention

Field of the Invention

5 The present invention relates to an inductor, more particularly, to a symmetrical stacked inductor made by a semiconductor process and applied to an inductor.

Description of the Related Art

10 The rapid development of communication technology forced the communication market to expand and requires more channels. Presently, portable communication devices have developed into devices with high frequency, light, thin, short, small and multiple functions so that the requirement of high accuracy, exactitude, credibility and modularizing is
15 needed. The effect of high frequency wireless communication focuses on the design of the radio frequency circuit, and the high frequency inductor of the radio frequency circuit requires a high quality factor, self-resonant frequency, low parasitic capacitance and high stability but it is hard to observe all factors during design.

20 Refer to Fig. 1, the conventional inductor 3, for example: a spiral inductor and a micro 3D inductor, applied to a symmetrical circuit such as an LC voltage control oscillator comprising two inductors 3, two capacitors, a close couple 7 and a topped device 9. The design of the LC voltage control oscillator 1 must be symmetrical. If not, two inductors have to be used for
25 maintaining symmetrical property of symmetrical circuit. The conventional design increased the area of the circuit layout, the cost and is ineffective in

decreasing phase noise.

Summary of the Invention

It is an object of the present invention to provide a symmetrical stacked
5 inductor which discloses a symmetrical inductor for decreasing the quantity of
inductors in design of a radio frequency circuit.

It is another object of the present invention to provide a symmetrical
stacked inductor which increases the quality of the inductor.

It is still another object of the present invention to provide a symmetrical
10 stacked inductor which decreases the phase noise of the radio frequency circuit.

The present invention comprises a plurality of conductive layers formed
out of symmetrical and geometric conductive layers, and each conductive layer
is placed between the inter-metal dielectric layers for isolating the conductive
layer. The conductive layer comprises at least one conductive line formed out
15 of a symmetrical and geometric, for example: rectangle, circle or others form,
conductive layer. Each inter-metal dielectric layer comprises a plurality of
via's for connecting upper and lower conductive layers.

Brief Description of the Drawings

20 The above and further objects, features and advantages of the invention
will become clear from the following more detailed description when read with
reference to the accompanying drawings in which:

Fig.1 is a circuit diagram using a conventional inductor in the construction
of an LC voltage control oscillator of the prior art;

25 Fig. 2 is a schematic view of a symmetrical stacked inductor according to
an embodiment of the present invention;

Fig. 3A is a symbol diagram of Fig. 2 according to an embodiment of the present invention;

Fig. 3B is a symbol diagram for using two conventional inductors of the prior art;

5 Fig. 3C is a circuit diagram for using the inductor applied to an LC voltage control oscillator according to an embodiment of the present invention;

Fig. 4A is a wave diagram of a spiral inductor of the prior art;

Fig. 4B is a wave diagram of a micro 3D inductor of the prior art;

Fig. 4C is a wave diagram of a symmetrical stacked inductor according to
10 an embodiment of the present invention;

Fig. 5 is a schematic view of a symmetrical stacked inductor according to another embodiment of the present invention;

Fig. 6 is a schematic view of symmetric stacked inductor according to another embodiment of the present invention;

15 Fig. 7 is a wave diagram for comparing the quality factor (Q) according to an embodiment of the present invention;

Fig. 8A is a schematic view of the voltage ratio=1:1 of a symmetrical stacked single chip transformer according to an embodiment of the present invention;

20 Fig. 8B is a schematic view of the voltage ratio= 1:n of a symmetrical stacked single chip transformer according to an embodiment of the present invention;

Fig. 9A is a schematic view of the voltage ratio=1:1 of a symmetrical stacked balun element according to an embodiment of the present invention;

25 Fig. 9B is a schematic view of the voltage ratio =1:n of a symmetrical stacked balun element according to an embodiment of the present invention;

Fig. 10A is a wave diagram of the gain response showing the balun element according to an embodiment of the present invention;

Fig. 10B is a wave diagram of the phase response showing the balun element according to an embodiment of the present invention;

5 Fig.11 is a schematic view of a symmetrical stacked inductor according to another embodiment of the present invention; and

Fig. 12 is a schematic view showing the symmetrical stacked inverting-type transformer according to an embodiment of the present invention.

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Detailed Description of the Preferred Embodiments

Refer to Fig. 2, the present invention comprises a symmetrical inductor 10 formed on the semiconductor and comprising a first conductive layer 12, a second conductive layer 14, a third conductive layer 16 and a fourth conductive layer 18 wherein each conductive layer 12, 14, 16, 18 being a symmetrical and geometric conductive layer and on a plane of the inter-metal dielectric layer of the semiconductor. The conductive layers 12, 14, 16, 18 are isolated respectively by an inter-metal dielectric layer, and each of them use at least a conductive line 20 forming a symmetrical and geometric conductive layer.

15 Further, the even conductive layers 14, 18 are the same as the odd conductive layers 12, 16 for decreasing parasitic capacitance generated. The form of the conductive layers 12, 14, 16, 18 could be, for example circular or other forms. A plurality of vias 22 are placed in the inter-metal dielectric layer for connecting the upper and lower side of neighboring conductive layers 12, 14, 16, 18 for electrical conduction. The first conductive layer 12 comprises a first port 24 and a second port 25, and the inductor 10 is a symmetrical shape

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whether from the view of the first port 24 or second port 25. Further, the middle side of the inductor 10 has a tapped apparatus 26.

Refer to Figs. 3A, 3B and 3C, the tapped apparatus 26 of the inductor 10 connects to ground or DC offset as show in Fig. 3A, and the construction is as
5 an inverting-type transformer (refer to Fig. 3B). Referring to Fig. 3C, the inductor 10 applied to an LC voltage control oscillator 27 comprising an inductor 10, a set capacitor 28, a closed couple circuit 29 and a tapped apparatus 26. When the inductor 10 is used in a symmetrical circuit, the LC voltage control oscillator 27 only uses one inductor 10 for replacing two
10 non-symmetrical and independent inductors 3 to decrease the design cost and circuit area.

Refer to Figs. 4A, 4B and 4C, a first wave line 30 is measured for the one port and the other port of the inductor being ground, and a second wave line 32 and the third wave line 34 are measured for the two ports. Refer to Figs. 4A
15 and 4B, the conventional inductor, spiral inductor and micro 3D inductor, could not totally overlap leading to bad symmetry properties. Refer to Fig. 4C, the wave lines 32, 34 almost overlap so that the inductor is a symmetrical inductor which can be applied to a symmetrical circuit. Therefore, the symmetrical inductor 10 applied in a symmetrical circuit only uses one symmetrical inductor
20 for replacing the conventional, two non-symmetrical and independent inductors to decrease the design cost and area.

Refer to Fig. 5, in another embodiment of the present invention, the inside of even conductive layer 36 of inductor 10 has a symmetrical and geometric even inside conductive layer 40 being the same as the odd conductive layer 38.
25 The even inside conductive layer 40 can not intersect with the even conductive layer 36. The even inside conductive layer 40 has a plurality of vias 42 in the

inter-metal dielectric layer and is parallel with the odd conductive layer 38. The outside of the odd conductive layer 38 has a symmetrical and geometric outside odd conductive layer 44 the same as the even conductive layer 36. The outside odd conductive layer 44 has a plurality of vias 42 in the inter-metal
5 dielectric layer and is parallel with the even conductive layer 36. The even inside conductive layer being parallel with the odd conductive layer 38 and odd outside conductive layer 44 being parallel with the even conductive layer 36 is called the multi level shunt for decreasing the series resistance.

Refer to Fig. 6, in another embodiment of the present invention, the inside
10 of even conductive layer 36 of the inductor 10 has a symmetrical and geometric even inside conductive layer 40 the same as the odd conductive layer 38. The even inside conductive layer 40 can not intersect with the even conductive layer 36. The even inside conductive layer 40 has a plurality of vias 42 in the inter-metal dielectric layer and is parallel with the odd conductive layer 38.
15 Further, cutting the odd outside conductive layer 44 improves the multi level shunt problem.

Refer to Fig. 7, with the fourth wave line 46 according to the embodiment of Fig. 2, the fifth wave line 48 according to the embodiment of Fig. 5, the sixth wave line 49 according to the embodiment of Fig. 6, the result are such
20 that the multi level shunt can decrease the series resistance and increase the quality factor (Q). In accordance with the even inside conductive layer 40 being parallel with the odd conductive layer 38 and odd outside conductive layer 44 being parallel with the even conductive layer 36, the parasitic capacitance is increased by the contacting area of the capacitor increased but
25 the quality factor (Q) is low so that improved multi level shunt decreases the voltage of the parasitic capacitance and increases the quality factor (Q).

Refer to Figs. 8A and 8B, a symmetrical stacked single chip transformer 50 comprises a first symmetrical stacked inductor 52 and a second symmetrical stacked inductor 54 wherein the first symmetrical stacked inductor 52 includes a first port 53, and the second symmetrical stacked inductor 54 includes a second port 55. Fig. 8A shows the voltage ratio = 1:1, and Fig. 8B shows the voltage ratio = 1:n.

Refer to Figs. 9A and 9B, in another embodiment of the present invention, the balun element 60 comprises a first symmetrical stacked inductor 62 and a second symmetrical stacked inductor 64 to form a symmetrical stacked single chip balun element 60 wherein the first symmetrical stacked inductor 62 includes a first port 63, and the second symmetrical stacked inductor 64 includes a second port 65 and a third port 66. Further, the middle of the balun element 60 has a tapped apparatus 68 for input of a DC offset. Fig. 9A shows the voltage ratio = 1:1, and Fig. 9B shows the voltage ratio = 1:n.

Refer to Figs. 10A and 10B, the wave diagrams show the gain and phase response of the balun element 60. The S21 curve 70 displays the gain response of the first port 63 and the second port 65, and the S31 curve 72 displays the gain response of the first port 63 and the third port 66. Further, the balun element 60 manifests less than 0.8 dB gain mismatch from 5.25 GHz to 6 GHz and phase error is about 4° for 5.25 GHz frequency band of interests.

Refer to Fig. 11, in another embodiment of the present invention, the symmetrical stacked inductor 80 comprises a first conductive layer 82 and a second conductive layer 83. The symmetrical stacked inductor 80 is different from the embodiment, refer to Fig. 2, which shows the every conductive layer including two conductive lines 84, and the conductive layer could stack n-layers according to the process. The higher inductance could get at same

area because the conductive layers 82, 83 have two conductive lines 84, and the coupling area increased between the conductive layers 82, 83 elevates the electromagnetic coupling effect being used to the symmetrical stacked transformer.

5 Refer to Fig. 12, which shows the view of a symmetrical stacked inverting-type transformer 85. The inverting-type transformer 85 comprises a symmetrical stacked inductor 80, and the middle side of the inductor 80 has a tapped apparatus 86. Further, the conductive layers 82, 83 of transformer 85 include two conductive lines 84 resulting in adding the coupling area and
10 elevating the electromagnetic effect. The conductive line 84 of the conductive layer gets the different gain response of the first port 88 and second port 89 (S21, k) according to the amount of the conductive line.

 The inductor 10 of the present invention is symmetrical so that the design of a radio frequency circuit only needs a symmetrical stacked inductor 10 to
15 replace the two conventional inductors for decreasing the circuit cost. Also, the middle of inductor 10 has a tapped apparatus 26 such as an invert transformer used in an LC voltage control oscillator 27 which decreases the area of the LC voltage control oscillator and lowers phase noise.

 Therefore, the foregoing is considered as illustrative only of the principles
20 of the invention. Further, since numerous modifications and changes will readily occur to those skilled in the art, it is not desired to limit the invention to the exact construction and operation shown and described, and accordingly, all suitable modifications and equivalents may be resorted to, falling within the scope of the invention.

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